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Peering Under the Hood: Investigating Next-generation Microelectronic Materials

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The drive toward smaller device dimensions and greater densities in high-performance CMOS (complementary metal–oxide–semiconductor) technology has led to the adoption of both novel designs and materials to achieve better performance. The challenges associated with incorporating these improvements present new opportunities for characterization of microelectronic technology, particularly at a submicron resolution. After a survey of existing techniques commonly employed in semiconductor manufacturing, examples will be given that demonstrate the needs for both highly localized and spatially averaged measurements. One such example involves strain engineering, which can improve carrier mobility but requires an understanding of the mechanical response of the device as a result of adjacent stressor structures. Synchrotron-based X-ray microbeam methods provide the capability to directly map the strain generated within silicon-on-insulator channels and their surrounding environment. A comparison of experimental data to mechanical modeling confirms that strain fields emanating from stressor features can extend large distances, leading to significant overlap in current designs. Another example is the detection of stress gradients generated at capping layer/metallization interfaces, where voiding phenomena such as electromigration can occur. *In situ* investigations of these buried interfaces can provide key information about conductor longevity and reliability.